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10/526,421	03/01/2005	Jeroen Anton Johan Leijten	NL02 0809 US	3287

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EXAMINER	
FAHERTY, COREY S	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,421	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/01/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed on 03/01/2005.

2. Claims 1-14 are pending in the application and have been examined.

Claim Objections

3. Claim 12 is objected to because of the following informalities: the claim recites character references in line 2 that have no meaning in the context of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 14 is rejected under 35 U.S.C. 101 because it is directed to a judicial exception rather than to a practical application of the judicial exception. A broad interpretation of the claim includes a software-only implementation, and for a judicial exception such as software to be patentable, it must have a practical application. That is, it must produce a useful, concrete and tangible result. Claim 14 is directed to a method but does not recite any method steps, and therefore does not produce a tangible result. For this reason, it fails to meet the requirements of 35 U.S.C. 101.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. For instance, claim 1 recites the limitation "said data processor being characterized by comprising controller means that are arranged for upon" in lines 4-5. The phrases "characterized by" and "arranged for" in this limitation are indefinite suggestions as to the limitations of the claim. Claim 3 recites the limitation "retrieving likewise restoring", the meaning of which is unclear. Other claims suffer from similar deficiencies. Applicant is requested to amend the claims such that their scope is readily and clearly defined.

9. Claim 2 recites the limitation "the earlier saved contents" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 11 recites the limitation "which may imply" in line 3. The meaning of this phrase is indefinite and makes defining the exact scope of the claim impossible.

11. Claim 12 recites the limitation "such handling of nested interrupts". It is not clear exactly what the phrase "such handling" refers to here, leaving the scope of the claim indefinite.

12. Claim 13 recites the limitation "an embedded data processor as claimed in Claim 1". However, no embedded data processor is claimed in claim 1, leaving the scope of the claim indefinite.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-3 and 5-7, 9 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al. (U.S. Patent 5,115,506), referenced from here forward as Cohen.

15. Regarding claims 1, 13 and 14, Cohen discloses a data processor comprising one or more functional units [col. 3, lines 23-25; the processor can be of the 68000-family, all of which include a functional unit], one or more register files [Fig. 1A], a data memory [Fig. 1A, memory stack], and a snapshot buffer which during the handling of an interrupt condition accommodates to save state information of various processor state elements in respective snapshot buffer elements [col. 8, lines 20-66; when an interrupt occurs, the register set that is used is switched so that the register data corresponding to each processing context is saved], said data processor being characterized by comprising controller means that are arranged for upon a subsequent interrupt condition that occurs during the handling of an actual interrupt condition saving the contents of said snapshot buffer elements in a data memory facility having a multibit access port facility [Fig. 1A; col. 8, lines 33-66; when a nested interrupt occurs, the data present in the multiple registers being used to execute the interrupt that is currently being handled is copied to a memory stack].

16. Regarding claim 2, Cohen discloses a data processor as claimed in Claim 1, wherein said controller means are arranged for upon completing the handling of an actual interrupt condition retrieving the earlier saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements [col. 9, lines 50-65; when processing completes the handling of a nested interrupt, the processor un-stacks from memory stack back to the register set any data associated with execution of the handling of an interrupt that was interrupted].

17. Regarding claim 3, Cohen discloses a data processor as claimed in Claim 2, wherein said controller means are arranged for upon said retrieving likewise restoring earlier saved state information of various processor state elements allowing said data processor to proceed with handling an earlier uncompleted interrupt, or, as the case may be to proceed with continuing a main thread of the processing [col. 10, lines 3-8; after interrupt processing completes, the processor switches back to using the original registers that were saved and continues normal operation].

18. Regarding claim 5, Cohen discloses a data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring their contents to said data memory facility [col. 8, lines 19-66; when an interrupt occurs, the data in registers corresponding to currently-executing interrupt handling code is saved to the stack memory; this data may be stored in different register sets, depending on the type of interrupt that is being handled; col. 8, lines 38-40; data may be stored from the prime registers to the stack; col. 8, lines 60-62; data may also be stored from the normal register set to the memory stack; Fig. 1A; the prime registers

are separate from the normal register set, so the data that is written to the external memory stack must be multiplexed to determine which registers are being written from].

19. Regarding claim 6, Cohen discloses a data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring their saved contents from said data memory facility [col. 9, lines 36-54; the processor may unstack data from the memory stack to different register sets in the processor, making a multiplexing operation essential to determine which will be written to].

20. Regarding claim 7, Cohen discloses a data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack [Fig. 1A; col. 7, line 14].

21. Regarding claim 9, Cohen discloses a data processor as claimed in claim 7, wherein write and read operations in said stack are executed at mutually exclusive instants in time [col. 8, lines 38-40; information associated with a first executing interrupt handler is stored to the stack when the first interrupt handler is interrupted; col. 9, lines 50-54; later, when a second interrupt handler that handles the interrupt that interrupted the first interrupt handler completes execution, the information associated with the first executing interrupt handler is retrieved from the stack].

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Petolino, Jr. et al. (U.S. Patent 5,958,041), referenced from here forward as Petolino.

24. Regarding claim 4, Cohen discloses that the state to be saved during interrupt processing includes data that is associated with the currently executing code [col. 8, lines 38-40], but does not explicitly disclose that this data includes latency data of current operations.

Petolino discloses a processor in which each load instruction has an associated latency prediction bit that is used to predict the proper latency period between the issuance of a load instruction and the issuance of any dependent instructions [col. 4, lines 25-30]. The purpose of the bit is to minimize the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include instruction latency data of current operations in the state that is saved during interrupt handling in the system of Cohen because Cohen discloses saving any data that is associated with currently executing code in response to an interrupt [col. 8, lines 38-40] and Petolino discloses associating an instruction latency bit with each load instruction [col. 4, lines 25-30] for the purpose of minimizing the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

25. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 7 above, and further in view of Patterson et al. (*Computer Organization & Design: The Hardware/Software Interface*), referenced from here forward as Patterson.

26. Regarding claim 8, Cohen discloses the data processor as claimed in claim 7, wherein the processor has a stack pointer [Fig. 1B], but does not explicitly disclose that the stack pointer allows multiple stack positions per snapshot. However, Cohen does disclose that, during the handling of an interrupt, an entire set of registers may be saved to the memory stack [col. 8, lines 40-44].

Patterson discloses a typical method for handling of a stack memory structure in a processor [pages 134-135; Figure 3.10]. The method includes decrementing the stack pointer using a subtract instruction (sub) and using store instructions (*sw*) to push registers onto the stack. Because multiple registers are pushed onto the stack, the value of the stack pointer is decremented by a value three times the size of each register. In this way, the multiple registers are pushed onto the stack at different stack locations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the stack pointer of Cohen allow multiple stack positions per snapshot because Cohen discloses that a single snapshot includes multiple registers [col. 8, lines 40-44] and Patterson discloses a typical method for handling a memory stack in which each register that is pushed onto the stack has its own stack location [pages 134-135; Figure 3.10]. Furthermore, allowing each register to have its own stack location gives the processor more versatility in determining which registers will be saved on the stack, potentially decreasing the processing time required to perform the save operation.

27. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Nguyen et al. (U.S. Patent 5,448,705), referenced from here forward as Nguyen.

28. Regarding claim 10, Cohen does not explicitly disclose that the snapshot buffer comprises shadow flipflops for storing snapshot information.

Nguyen discloses a method for handling traps in a processor in which, when a trap is encountered, a number of shadow registers are shifted to the foreground to be used by the trap handling routine and the corresponding foreground registers are shifted into the background to be saved as shadow registers [col. 3, lines 54-64]. The purpose of using shadow registers to construct a snapshot buffer in the processor is so the trap handler has a set of registers immediately available for use without any need to be concerned about destroying data needed for the main instruction stream [col. 3, lines 61-64].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use shadow flipflops to store snapshot information in the processor of Cohen because Nguyen discloses using shadow registers to hold snapshot information during a trap [col. 3, lines 54-64] and teaches that doing so allows the trap handler to immediately access registers without being concerned about destroying data needed for the main instruction stream, because that data is stored in the new shadow registers [col. 3, lines 54-64].

29. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Lang et al. (*Individual Flip-Flops with Gated Clocks for Low Power Datapaths*), referenced from here forward as Lang.

30. Regarding claim 11, Cohen discloses the data processor as claimed in claim 1, wherein the processor has a stack pointer [Fig. 1B], but does not explicitly disclose that the flipflops comprising the stack pointer are clocked only during stack pointer updates.

Lang discloses a method for operating flipflops in which the flipflops are only clocked when the flipflop must change [section 1, paragraph 3]. The purpose of doing this is to reduce the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clock the flipflops comprising the stack pointer in Cohen only during stack pointer updates because Lang discloses a technique in which flipflops are clocked only when the flipflop must change values [section 1, paragraph 3] and teaches that using this technique reduces the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Shen et al. (*Modern Processor Design: Fundamentals of Superscalar Processors*), referenced from here forward as Shen.

32. Regarding claim 12, Cohen discloses the data processor as claimed in claim 1, but does note explicitly disclose that it has a plurality of issue slots and that a single issue slot handles the processing of nested interrupts. However, Cohen does disclose that the handling of nested interrupts is done by writing to and reading from a stack memory structure [col. 8, lines 54-56; col. 9, lines 36-40].

Shen discloses a processing technique having multiple parallel issue units, or reservation stations [page 175, Figure 4-26]. There is a unique reservation station reserved for all load and store instructions such as those used by Cohen to perform nested interrupt operations [page 175, Figure 4-26; reservation station coupled to the load/store unit]. It is advantageous to have a separate reservation station assigned to each functional unit because it allows for smaller

reservation stations and a large reservation station can be quite complex to implement in a processor [page 177, paragraph 3].

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of issue slots, one of which is used to handle the processing of nested interrupts, in the system of Cohen because Shen discloses a processor having a plurality of parallel issue units [page 175, Figure 4-26] wherein one of the reservation stations is assigned to handle all memory instructions such as those used by Cohen [col. 8, lines 54-56; col. 9, lines 36-40] to perform nested interrupt operations [page 175, Figure 4-26; reservation station coupled to the load/store unit]. Furthermore, it is advantageous to have a separate reservation station assigned to each functional unit because it allows for smaller reservation stations and a large reservation station can be quite complex to implement in a processor [page 177, paragraph 3]. The issuing methods disclosed in Shen are well known and common in the computer arts and their application to the processor in Cohen would be obvious in the design of a high-speed superscalar processor.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art is closely related to the subject matter of the instant application and should be fully considered in any reply to this office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty
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CF

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